UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/316,560	05/24/99	DURANTON M	PHF-99.540V

TM02/0404

CORPORATE PATENT COUNSEL
US PHILIPS CORPORATION
580 WHITE ROAD
TARRYTOWN NY 10591

EXAMINER	
BRAGDON, R	
ART UNIT	**PAPER NUMBER**
2185	6

DATE MAILED: 04/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/316,560	Applicant(s) DURANTON, MARC	
	Examiner Reginald G. Bragdon	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *15 December 1999 and 08 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 12-15-1999 has been considered. Please see the attached PTO-1449(s).

2. The Examiner acknowledges receipt of the PCT Search Report received 9-8-2000.

Drawings

3. The drawings have been approved by the Office draftsperson and the Examiner.

Claim Objections

4. Claims 1-5 are objected to because of the following informalities:

As per claim 1, lines 12 and 15, "in" should be --for-- since the memory circuits are not disclosed as generating a write or read address, but instead the MCU generates a write or read address for the memory circuits.

As per claim 4, lines 6 and 8, "in" should be --for-- since the memory circuits are not disclosed as generating a write or read address, but instead the MCU generates a write or read address for the memory circuits.

As per claim 5, lines 11 and 13, "in" should be --for-- since the memory circuits are not disclosed as generating a write or read address, but instead the MCU generates a write or read address for the memory circuits.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Torii et al. (4,734,850).

As per claims 1, 4, and 5, Torii et al. teaches a data processing system including a plurality of execution units (E-units 1 and 6 in figure 1), which represent a "first processor" and a "second processor". A "memory system" is shown in figure 2, including memory banks 47, 48 ("plurality of memory circuits"). A mode indicating circuit 41 ("master controller") provides a signal for repetitively indicating at a constant interval a write mode to banks 47, 48. See column 3, lines 26-43. A read/write control circuit 100 ("control unit") generates a write address from a write control circuit 42 for write data ("selecting a first memory...by the first processor"; see column 4, line 60, to column 5, line 22) and a read address from read control circuit 43 for read data ("selecting a second memory...by the second processor"; see column 6, line 64 to column 7,

line 11). Furthermore, Torii et al. teaches writing to one bank 47 simultaneously with reading from the other bank 48, and visa versa. See column 7, lines 46-52.

As per claim 2, Torii et al. teaches a write counter and a read counter for generating addresses. See claim 18, for example, and figures 4 and 5.

As per claim 3, Torii et al. teaches a write request input, WREQ, ("NXT_W") and a read request input, RREQ, ("NXT_R"). See column 4, lines 2-13, and column 6, lines 39-41.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Csoppenszky et al. (5,852,608) teaches a dual-port memory located between two systems.

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 305-9051, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2185

RGB
11-Feb-01